High Reliability IP for Automotive and Datacenter Applications

Analog Bits

ABSTRACT

Analog Bits, the leading provider of mixed-signal IP solutions, will present on High Reliability for IP in advanced process nodes including TSMC's 7nm process. Analog Bits' IP products are used in billions of devices, resulting in: lower power products, reduced design risk and more competitive offerings. This presentation will focus on Automotive and Datacenter applications, where reliability of IP solutions is critical to commercial success.

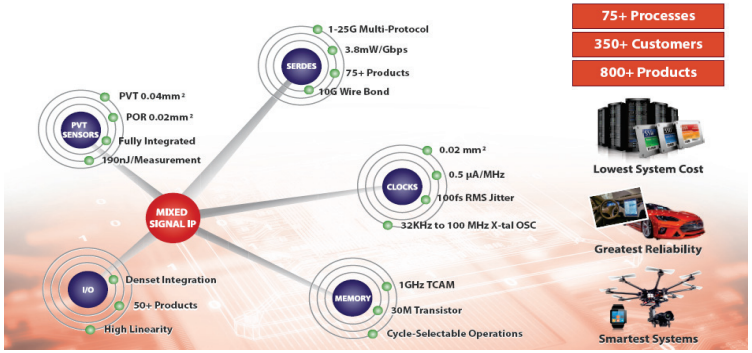
ANALOG BITS

High Reliability IP for Automotive and Datacenter Applications

Mahesh Tirupattur
Executive VP

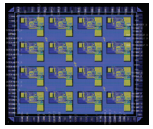
Broadest Portfolio of Differentiated IP

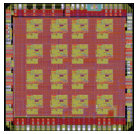
Billions in Silicon

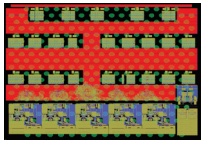


Advanced Technology Leadership with **TSMC**

16nm FF IP Shipping in Production and 7nm Pre-Production


16FFC Test Chip


Automotive Grade 16FFC Test Chip


16FFC Multi-Lane SERDES Test Chip

- Multiple products on 16nm in **Mass Production** for Smart Phones
- Demonstrated **lowest power** 1-16G SERDES test chips in 16FF+
- 16FFC test chips with PLL and Sensor IP's **working silicon demonstrated**
- 16FFC **Automotive-grade** PLL, Sensor and Xtal OSC test-chip taped-out in August shuttle
- 16FFC 1-22.5G Enterprise Class SERDES **working silicon demonstrated**
- 16FFC 1-10G Ultra low power SERDES **working silicon demonstrated**
- 7nm FF early partner with TSMC
- 7nm PLL and Sensors **Test Chip taped-out** in May 2017
- Low Power SERDES Test Chip in 7FF+ Q1-18

Higher Reliability Considerations for Automotive

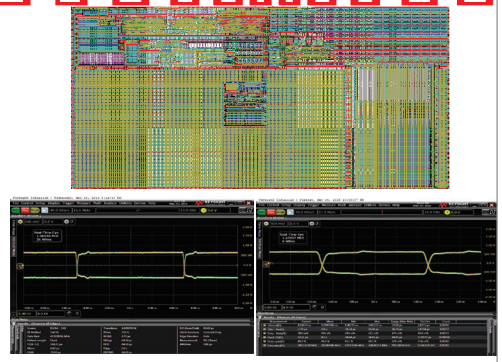
- With Multi-CPU designs, **sensors** are getting super-critical
- **Temperature range extended** up to 150C – Grade 1
- Performance and power-centric designs for both **ADAS** and **Infotainment**
- Extensive aging analysis to assure **endurance to harsher environments**
- IP has to be highly **testable** and **robust** against non-testable parameters
- **Automotive-Class** Documentation

Design Considerations for Datacenter Applications

- Big Data Disruption with **2.5 Quintillion Bytes** of data per day
- Higher BW of data in and out of chip with **highest efficiency and lowest latency**
- Advent of air-cooled Datacenter – **lowest power and smallest area**
- Design considerations are evolving – **newer SERDES standards** and data-rates
- High integration of SERDES macros – **150+ Lanes on a small SoC** die

Low Power, Small Form Factor **TSMC 16FFC PLL**

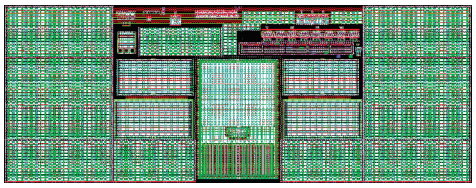
- Silicon-proven in Datacenter SOC's
- Specs
  - VCO Freq. > 6.4GHz
  - Typ Power < 3mA
  - Area 0.013 sq.mm
  - Temp: -40 to 125C
- Automotive enhancements
  - Improved EM at 150C
  - Rigorous verification of digital elements
    - Asymmetric BTI Aging Sims
  - Clock Tree quality checking
    - PMOS/NMOS skew testing
  - Automotive-class documentation of testing



6.4GHz VCO with ref clock of 200/50MHz @ 125C

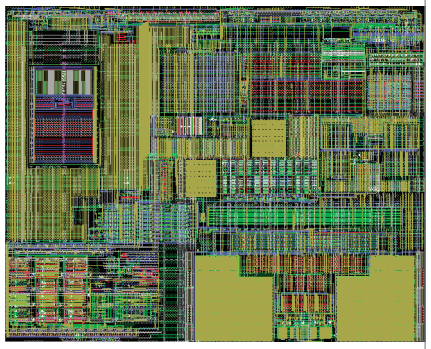
TSMC 16FFC Low Noise Oscillator Pads

- Designed for Automotive-class
  - Supports many industry standard crystals in the 20-40MHz range
  - Oscillation Mode: Fundamental
  - Power down option for IDDQ testing
  - Bypass mode option for logic testing
  - Self-contained ESD
- Design Considerations
  - Extensive Monte Carlo and aging simulations
  - Automotive class documentation of design and testing



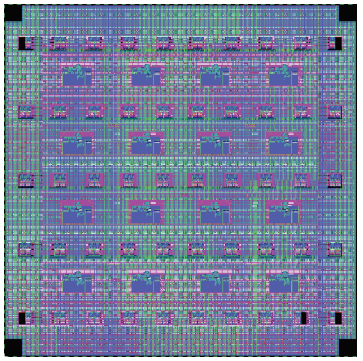
Fully Integrated **TSMC 16FFC** PVT Sensor

- Silicon-proven in Datacenter SOC's
- Automotive-grade enhancements
  - Grade 1 Class – 150C
    - EM and Leakage considerations
  - Additional process corner sampling
    - P/N process corner sampling
    - Multiple channel length sampling
    - Thick-oxide (1.8V) device sampling
  - Robust design verification of mixed-signal blocks
  - Statistical circuit validation
    - Extensive Monte Carlo up to 6 sigma
    - Asymmetric BTI aging sims



TSMC 7nm Test-Chip

- Taped-out May 2017
- High Performance Low Power PLL
  - VCO Freq. > 8 GHz
  - Typ Power < 4 mA
  - Area 0.008 sq.mm
  - Temp: -40 to 125C
  - 4LM
- Numerous Sensors scattered across the Die
- Silicon Characterization – Q4 2017



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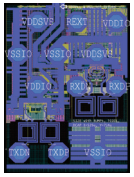
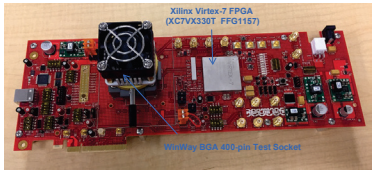
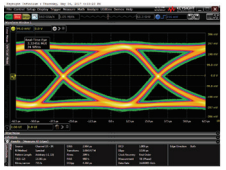
TSMC 16FFC: Enterprise Class 1-25G SERDES
Multiprotocol: XFI,10GKR, PCIe4, SAS4



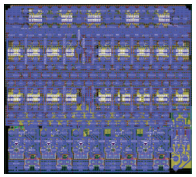
1-22.5G SERDES PMA



1-22.5G SERDES Test Board



16Gb/s TX Eye Diagram



5L SERDES Test Chip

Data Rate (Gbps)	Total Power (mW/lane)	Power (mW/Gbps/lane)
16	98.25	6.9

22.5Gb/s TX Eye Diagram

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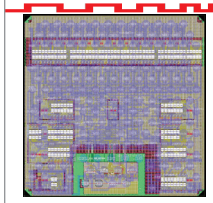
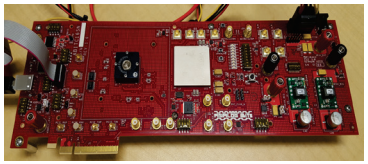
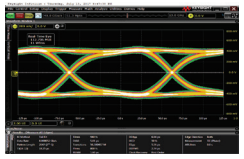
TSMC 16FFC: Consumer/Automotive-Class 1-10G
Multiprotocol: SGMII, XAUI/RXAUI, SATA3, PCIe3



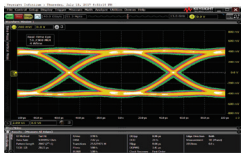
Data Rate (Gbps)	Total Power (mW/lane)	Power (mW/Gbps/lane)
5	30.85	6.17
8	34.31	4.29



5Gb/s TX Eye Diagram



8Gb/s TX Eye Diagram



10Gb/s TX Eye Diagram

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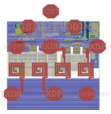
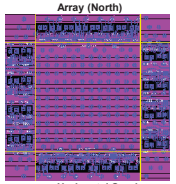
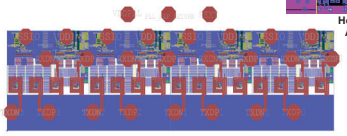
Integrated, Flexible Bump Pitch Including **TSMC** Copper Pillars, Multiple Orientations

Vertical Orientation (4-lane)



Single Lane





Horizontal Orientation (4-lane)

Allows SERDES to be Placed Anywhere on SoC

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FinFET SERDES Development Status and Plan

- **1-16G SERDES in TSMC 16FF+**
  - **Available now** (silicon proven) - Ready for customer tape-out
- **1-10G Ultra-low area and low-power SERDES in TSMC 16nm/12FFC**
  - **Available now** (silicon proven) - Ready for customer tape-out
- **1-22.5G-class SERDES in TSMC 16FFC**
  - **Available now** (silicon proven) - Ready for customer tape-out

- **1-16G SERDES in 7FF+**
  - Test Chip Tape-out in Feb. 2018
  - **Ready for early customer** engagements now
- **1-32G class SERDES in 7FF+**
  - Test Chip Tape-out in June 2018
  - **Ready for early customer** engagements now

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A Lasting Partnership

35+ Processes, 300+ Customers, 600+ IP Products

13+ Years of Partnership including FinFET

ANALOG BITS **TSMC**

Wide range of processes supported

CL025, CL018G. CL018LV, CL018IMG, CL015G, CL015LV, CL013G, CL013LV CL013LVOD, CL011LV, CL011G, CLN90G, CLN90GT, CLN90LP, CLN80GC, CLN65LP, CLN65GP, CLN55GP, CLN55LP, CLN40G, CLN40LP, LLN40ULP, CLN28HP, CLN28HPL, CLN28HPM, CLN28HPC, CLN28HPC+, CLN20SOC, 16FF+GL, 16FF+LL, 16FFC, 12FFC, 7FF, 7FF+

Highest degree of collaboration on Test-Chips in FinFets including Split Lots for 5 Corners to meet Automotive and Datacenter Needs

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Conclusions

- 16FFC IP's are **production proven** in Consumer and Datacenter applications
- 16FFC IP's are being tuned for **Automotive Grade Performance**
- 7FF IP's are in pre-production and in parallel **optimized for Automotive Grade**
- SERDES products are being optimized on 2 Tracks for 16FFC and 7FF
  - **High-performance** and optimized for High Loss channels such as Datacenters
  - **Low-power optimized** for Consumer and Automotive Applications

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